

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently amended) An equalization circuit to receive a plurality of
2 input symbols and to generate an output signal wherein the output signal is
3 representative of a transmitted symbol, the equalization circuit comprising:
4 a first data slicer having a plurality of inputs and an output, wherein a first
5 input is adapted to receive the plurality of input symbols and a second input is
6 adapted to receive a first slicer level, and wherein the first data slicer outputs a
7 first or second value based on the amplitude of the input symbol relative to the
8 first slicer level;
9 a second data slicer having a plurality of inputs and an output, wherein a
10 first input of the second data slicer is adapted to receive the plurality of input
11 symbols and a second input of the second data slicer is adapted to receive a
12 second slicer level, and wherein the second data slicer outputs the first or second
13 value based on the amplitude of the input symbol relative to the second slicer
14 level; and
15 logic circuitry, coupled to the first and second data slicers, to output a
16 signal having either a first or second logic level wherein the first logic level is
17 associated with the first value and the second logic level is associated with the
18 second logic level, and wherein:
19 if the data slicers output the same value, the logic circuitry
20 outputs the logic level that is associated with the value output by
21 the data slicers; and

22 | if the data slicers output different values, the logic circuitry
23 | outputs the complement of the logic level of the immediately
24 | preceding input symbol; and
25 | marginizing circuitry to measure the value of an error signal
26 | of a level sampling point.

1 2. (Original) The equalization circuit of claim 1 wherein the first and
2 second data slicers each include at least one voltage comparator.

1 3. (Original) The equalization circuit of claim 2 wherein the first and
2 second data slicers each include a plurality of serially coupled sense amplifiers.

1 4. (Original) The equalization circuit of claim 1 further including adaptive
2 circuitry, coupled to the first data slicer, to determine the first slicer level during
3 operation of the equalization circuit and to provide the first slicer level to the first
4 data slicer.

1 5. (Currently amended) A receiver, coupled to a communications channel,
2 to receive a plurality of input symbols transmitted by a transmitter, and to generate
3 an output signal that is representative of each transmitted symbol, the receiver
4 comprising:
5 equalization circuitry, coupled to the communications channel to receive
6 the plurality of input symbols, the equalization circuitry including:
7 a first data slicer having a plurality of inputs and an output, wherein a first
8 input is adapted to receive the plurality of input symbols and a second input is
9 adapted to receive a first slicer level, and wherein the first data slicer outputs a
10 first or second value based on the amplitude of the input symbol relative to the
11 first slicer level;

12 a second data slicer having a plurality of inputs and an output, wherein a
13 first input of the second data slicer is adapted to receive the plurality of input
14 symbols and a second input of the second data slicer is adapted to receive a
15 second slicer level, and wherein the second data slicer outputs the first or second
16 value based on the amplitude of the input symbol relative to the second slicer
17 level;

18 logic circuitry, coupled to the first and second data slicers, to output a
19 signal having either a first or second logic level wherein the first logic level is
20 associated with the first value and the second logic level is associated with the
21 second logic level, and wherein:

22 if the data slicers output the same value, the logic circuitry
23 outputs the logic level that is associated with the value output by
24 the data slicers; and

25 if the data slicers output different values, the logic circuitry
26 outputs the complement of the logic level of the immediately
27 preceding input symbol;

28 marginizing circuitry to measure the value of an error signal of a level sampling
29 point; and

30 a memory, coupled to the second input of each data slicers, wherein the
31 memory stores information which is representative of the first and second slicer
32 levels.

1 6. (Original) The receiver of claim 5 further including adaptive circuitry,
2 coupled to the second input of each data slicers, wherein the adaptive circuitry
3 adjusts the first and second slicer levels in accordance with the performance of the
4 receiver.

1 7. (Original) The receiver of claim 5 further including adaptive circuitry,
2 coupled to the second input of the first data slicer, wherein the adaptive circuitry

3 changes the first data slicer level based on an upper edge and a lower edge of a
4 receive eye of the first data slicer.

1 8. (Original) The receiver of claim 7 further including margining circuitry,
2 coupled to the adaptive circuitry, wherein the margining circuitry determines the
3 upper inner edge and the lower inner edge of the receive eye of the first data
4 slicer.

1 9. (Original) The receiver of claim 8 wherein the margining circuitry
2 includes a margining slicer having a plurality of inputs and an output, wherein a
3 first input of the margining slicer is adapted to receive the plurality of input
4 symbols and a second input is adapted to receive a margining slicer level, and
5 wherein the margining slicer outputs a first or second value based on the
6 amplitude of the input symbol relative to the margining slicer level.

1 10. (Original) The receiver of claim 9 wherein the margining circuitry
2 includes reference level adjustment circuitry to generate the margining slicer level.

1 11. (Original) The receiver of claim 10 wherein the reference level
2 adjustment circuitry generates margining slicer levels that vary according to the
3 margining algorithm.

1 12. (Original) The receiver of claim 7 further including adaptive circuitry,
2 coupled to the second input of the second slicer, wherein the adaptive circuitry
3 changes the second slicer level based on an upper edge and a lower edge of a
4 receive eye of the second slicer.

1 13. (Original) The receiver of claim 12 further including margining
2 circuitry, coupled to the adaptive circuitry, wherein the margining circuitry
3 determines the location of the upper inner edge and the lower inner edge of the
4 receive eyes of the first and second slicer.

1 14. (Original) The receiver of claim 12 wherein the margining circuitry
2 includes a margining slicer having a plurality of inputs and an output, wherein a
3 first input of the margining slicer is adapted to receive the plurality of input
4 symbols and a second input is adapted to receive a margining slicer level, and
5 wherein the margining slicer outputs a first or second value based on the
6 amplitude of the input symbol relative to the margining slicer level.

1 15. (Original) The receiver of claim 14 wherein the margining circuitry
2 includes reference level adjustment circuitry to generate the margining slicer level.

1 16. (Original) The receiver of claim 15 wherein the reference level
2 adjustment circuitry generates margining slicer levels that vary according to the
3 margining algorithm.

1 17. (Currently amended) The receiver of claim 15 further including:
2 | a first data-phase slicer having a plurality of inputs and an output, wherein
3 a first input is adapted to receive the plurality of input symbols and a second input
4 is adapted to receive a first slicer level, and wherein the first data slicer outputs a
5 first or second value based on the amplitude of the input symbol relative to the
6 first slicer level;
7 | a second data-phase slicer having a plurality of inputs and an output,
8 wherein a first input of the second data slicer is adapted to receive the plurality of
9 input symbols and a second input of the second data slicer is adapted to receive a

10 second slicer level, and wherein the second data slicer outputs the first or second
11 value based on the amplitude of the input symbol relative to the second slicer
12 level;
13 | margining circuitry to measure the value of an error signal of a level-phase
14 sampling point; and
15 adaptive circuitry, coupled to margining circuitry and the second input of
16 the first slicer, wherein the adaptive circuitry changes the first slicer level based
17 on the value of the error signal.

1 18. (Original) The receiver of claim 17 wherein the margining circuitry
2 includes a margining slicer having a plurality of inputs and an output, wherein a
3 first input of the margining slicer is adapted to receive the plurality of input
4 symbols and a second input is adapted to receive a margining slicer level, and
5 wherein the margining slicer outputs a first or second value based on the
6 amplitude of the input symbol relative to the margining slicer level.

1 19. (Currently amended) A receiver, coupled to a communications
2 channel, to receive a plurality of input symbols transmitted by a transmitter, and to
3 generate an output signal that is representative of each transmitted symbol, the
4 receiver comprising:
5 equalization circuitry, coupled to the communications channel to receive
6 the plurality of input symbols, the equalization circuitry including:
7 a first data slicer having a plurality of inputs and an output, wherein a first
8 input is adapted to receive the plurality of input symbols and a second input is
9 adapted to receive a first slicer level, and wherein the first data slicer outputs a
10 first or second value based on the amplitude of the input symbol relative to the
11 first slicer level;
12 a second data slicer having a plurality of inputs and an output, wherein a
13 first input of the second data slicer is adapted to receive the plurality of input

14 symbols and a second input of the second data slicer is adapted to receive a
15 second slicer level, and wherein the second data slicer outputs the first or second
16 value based on the amplitude of the input symbol relative to the second slicer
17 level;
18 logic circuitry, coupled to the first and second data slicers, to output a
19 signal having either a first or second logic level wherein the first logic level is
20 associated with the first value and the second logic level is associated with the
21 second logic level, and wherein:
22 if the data slicers output the same value, the logic circuitry
23 outputs the logic level that is associated with the value output by
24 the data slicers; and
25 if the data slicers output different values, the logic circuitry
26 outputs the complement of the logic level of the immediately
27 preceding input symbol;
28 margining circuitry, including at least one margining slicer, to determine
29 the value of an error signal of a level sampling point at least one performance
30 parameter of the receiver; and
31 adaptive circuitry, coupled to the margining circuitry and the second input
32 of the first data slicer, wherein the adaptive circuitry adjusts the first slicer level
33 based on the at least one performance parameter.

1 20. (Original) The receiver of claim 19 wherein the at least one
2 performance parameter of the receiver includes an upper inner edge and a lower
3 inner edge of a receive eye of the first data slicer.

1 21. (Original) The receiver of claim 19 wherein the at least one
2 performance parameter of the receiver includes an upper edge and a lower edge of
3 a receive eye of the second data slicer.

1 22. (Original) The receiver of claim 19 wherein the at least one
2 performance parameter of the receiver includes error signal of a phase sampling
3 point.

1 23. (Original) The receiver of claim 19 wherein the margining slicer
2 includes a plurality of inputs and an output, wherein a first input of the margining
3 slicer is adapted to receive the plurality of input symbols and a second input is
4 adapted to receive a margining slicer level, and wherein the margining slicer
5 outputs a first or second value based on the amplitude of the input symbol relative
6 to the margining slicer level.

1 24. (Original) The receiver of claim 23 wherein the margining circuitry
2 includes reference level adjustment circuitry to generate the margining slicer level.

1 25. (Original) The receiver of claim 24 wherein the reference level
2 adjustment circuitry generates margining slicer levels that vary according to the
3 margining algorithm.

1 26. (Original) The receiver of claim 19 wherein the first, second and
2 margining data slicers each include a plurality of serially coupled sense amplifiers.